IN THE CLAIMS

1-22. (canceled)

23. (previously presented) A method of executing a program with a processor, the processor being capable of executing a set of instructions, comprising:

providing an original instruction from a sequence of instructions comprising a program stored in a memory;

generating an address from the original instruction;

generating a jump and link instruction to the address, the jump and link instruction comprising an instruction for the processor to execute instructions at the address and then return to the instruction following the original instruction in the program;

determining whether the original instruction is a member of the set of instructions;

selecting the jump and link instruction or the original instruction based on the result of the step of determining; and

providing the selected instruction to the processor;

wherein the step of determining whether the original instruction is a member of the set of instructions is performed in parallel with generating the address and generating the jump and link instruction.

24. (original) The method of claim 23 further including providing the selected instruction to an instruction cache of the processor.

25. (original) The method of claim 24 wherein the step of providing an original instruction includes retrieving the instruction from a memory.

26-30. (canceled)

31. (previously presented) A system for processing computer instructions comprising:

a source of complex and simple instructions, the simple instructions being capable of being executed by the processor and the complex instructions not being capable of being executed by the processor,

a complex instruction detector connected to the source and an instruction selector, the complex instruction detector receiving computer instructions from the source and providing a value indicative of whether a received instruction is complex or simple,

an address generator connected to the source and a jump instruction generator, the address generator receiving computer instructions from the source and, if a received instruction is complex, providing an address in a memory containing emulation instructions to the jump instruction generator, whereby the emulation instructions are simple instructions and emulate the intended function of the complex instruction,

the jump instruction generator being connected to the address generator and the instruction selector, the jump instruction generator receiving addresses from the address generator and providing jump and link instructions to the addresses,

the instruction selector being connected to the jump instruction generator and the complex instruction detector such that the instruction selector provides a jump and link instruction from the jump instruction generator if the instruction received from the source is complex, or provides the instruction if the instruction received from the source is simple, and

a processor for receiving the instructions from the instruction selector;

wherein the complex instruction detector is configured to operate on the received instruction in parallel with the address generator and the jump instruction generator operating on the received instruction.

32. (original) The system of claim 31 further comprising an instruction cache disposed between the instruction selector and the processor.

33. (original) The system of claim 31 wherein the address generator provides a first address in response to a first complex instruction and a second address in response to a second instruction, the first and second addresses being different.

34. (original) The system of claim 31 wherein the complex instruction detector uses routines associated with reserved instruction exceptions.

35. (previously presented) A system for processing a computer instruction from a source of such instructions, the system comprising:

a complex instruction detector being operable to accept computer instructions from the source and to determine whether each instruction is a complex instruction on an instruction by instruction basis;

an address generator being operable to accept computer instructions from the source and to output an address for each of the computer instructions based on the respective computer instruction;

a jump instruction generator in operative communication with the address generator, the jump instruction generator being operable to receive information from the address generator and to output an instruction to jump to the address

output from the address generator based upon the information; and

an instruction selector in operative communication with the jump instruction generator, the source, and the complex instruction detector, the instruction selector being operable to output either the computer instruction from the source or the instruction from the jump instruction generator depending upon the determination by the complex instruction detector;

wherein the complex instruction detector is configured to operate on the computer instructions in parallel with the address generator operating on the computer instructions and the jump instruction generator operating on the information received from the address generator.

36-37. (canceled)